WHAT IS CLAIMED IS:

1. A laminated capacitor comprising:

a capacitor body having first and second major surfaces and including a laminated stack of a plurality of dielectric layers, at least a pair of a first and second internal electrodes opposed to each other with at least one of the dielectric layers being disposed therebetween;

a plurality of first feedthrough conductors perforating through at least one of the dielectric layers provided within the capacitor body, the first feedthrough conductors being electrically insulated from the second internal electrodes and electrically connected to the first internal electrodes; and

a plurality of second feedthrough conductors perforating through the capacitor body and provided within the capacitor body, the second feedthrough conductors are electrically insulated from the first internal electrodes and are electrically connected to the second internal electrodes, the first and second feedthrough conductors are arranged to offset the magnetic fields induced by the electric current flowing through the internal electrodes;

a plurality of first external terminal electrodes arranged so as to correspond to the respective first feedthrough conductors and electrically connected to respective ones of the first feedthrough conductors; and

a plurality of second external terminal electrodes, which are arranged to correspond to respective ones of the second feedthrough conductors and electrically connected to respective ones of the second feedthrough conductors; wherein

the first external terminal electrodes are located at least on the first major surface of the capacitor body and extend substantially parallel to the internal electrodes, and the second external terminal electrodes are located on both the first major surface and the second major surface in opposed relation to the first major surface.

2. A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 2×10^{-3} mm^2.

3. A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

4. A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

5. A laminated capacitor according to Claim 1, wherein

the first external terminal electrodes are disposed on both the first major surface and the second major surface of the capacitor body.

6. A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross sectional area of at least about 2×10^{-3} mm^2.

7. A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

8. A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

9. A laminated capacitor according to Claim 1, wherein solder bumps are provided on the first and second external terminal electrodes.

10. A laminated capacitor according to Claim 1, wherein the laminated capacitor defines a decoupling capacitor.

11. A wiring connection structure of a decoupling capacitor to be connected to a power supply circuit for a MPU chip provided in a microprocessing unit, the decoupling capacitor comprising:

a capacitor body having first and second major surfaces opposed to each other;

feedthrough conductors disposed within the capacitor body and arranged to perforate from the first major surface to the second major surface; and

at least one of power supply lines and signal lines connected to the MPU chip are grounded to a mother board via the feedthrough conductors.

12. A wiring connection structure of a decoupling capacitor according to Claim 11, wherein the decoupling capacitor includes:

a capacitor body having first and second major surfaces and including a laminated stack of a plurality of dielectric layers, at least a pair of a first and second internal electrodes opposed to each other with at least one of the dielectric layers being disposed therebetween;

a plurality of first feedthrough conductors perforating through at least one of the dielectric layers provided within the capacitor body, the first

feedthrough conductors being electrically insulated from the second internal electrodes and electrically connected to the first internal electrodes; and

a plurality of second feedthrough conductors perforating through the capacitor body and provided within the capacitor body, the second feedthrough conductors are electrically insulated from the first internal electrodes and are electrically connected to the second internal electrodes, the first and second feedthrough conductors are arranged to offset the magnetic fields induced by the electric current flowing through the internal electrodes;

a plurality of first external terminal electrodes arranged so as to correspond to the respective first feedthrough conductors and electrically connected to respective ones of the first feedthrough conductors; and

a plurality of second external terminal electrodes, which are arranged to correspond to respective ones of the second feedthrough conductors and electrically connected to respective ones of the second feedthrough conductors; wherein

the first external terminal electrodes are located at least on the first major surface of the capacitor body and extend substantially parallel to the internal electrodes,

and the second external terminal electrodes are located on both the first major surface and the second major surface in opposed relation to the first major surface .

13. A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 2×10^{-3} mm^2.

14. A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

15. A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

16. A wiring connection structure of a decoupling capacitor according to Claim 12, wherein the first external terminal electrodes are disposed on both the first major surface and the second major surface of the capacitor body.

17. A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross sectional area of at least about 2×10^{-3} mm^2.

18. A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

19. A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

20. A wiring connection structure of a decoupling capacitor according to Claim 12, wherein solder bumps are provided on the first and second external terminal electrodes.

21. A wiring connection structure of a decoupling capacitor according to Claim 11, wherein a hot side of the power supply circuit is connected to the first external terminal electrode.

22. A wiring board package apparatus comprising:

a wiring board;

a MPU chip of a microprocessing unit mounted on the wiring board;

wiring conductors at a hot-side thereof for a power source arranged to supply electricity to the MPU chip and ground side wiring conductors; and

a laminated capacitor having first and second major surfaces, the laminated capacitor including a capacitor body having first and second major surfaces and including a laminated stack of a plurality of dielectric layers, at least a pair of a first and second internal electrodes opposed to each other with at least one of the dielectric layers being disposed therebetween, a plurality of first feedthrough conductors perforating through at least one of the dielectric layers provided within the capacitor body, the first feedthrough conductors being electrically insulated from the second internal electrodes and electrically connected to the first internal electrodes, and a plurality of second feedthrough conductors perforating through the capacitor body and provided within the capacitor body, the second feedthrough conductors are electrically insulated from the first internal electrodes and are electrically connected to the second internal electrodes,

the first and second feedthrough conductors are arranged to offset the magnetic fields induced by the electric current flowing through the internal electrodes, a plurality of first external terminal electrodes arranged so as to correspond to the respective first feedthrough conductors and electrically connected to respective ones of the first feedthrough conductors, a plurality of second external terminal electrodes, which are arranged to correspond to respective ones of the second feedthrough conductors and electrically connected to respective ones of the second feedthrough conductors; wherein the first external terminal electrodes are located at least on the first major surface of the capacitor body and extend substantially parallel to the internal electrodes, and the second external terminal electrodes are located on both the first major surface and the second major surface in opposed relation to the first major surface, the laminated capacitor being arranged on the wiring board such that the first major surface is directed toward the wiring board side and the second major surface is directed toward the outside of the package, the first external terminal electrodes at the first major surface side being electrically connected to the wiring conductors at the hot side for the power source, and the second external terminal electrodes at the first major surface side being electrically connected to the ground side wiring conductors.

23. A wiring board package apparatus according to Claim 22, wherein the MPU chip is mounted on the first substrate surface of the wiring board, a cavity having an opening along the second substrate surface opposed to the first substrate surface, and the second major surface is directed toward the opening side of the cavity, the second major surface being on the same level as the second substrate surface.

24. A wiring board according to Claim 22, wherein the MPU chip comprises a plurality of terminals arranged to have substantially the same pitch as the pitch of the arrangement of the first and second external terminal electrodes of the laminated capacitor.